**Amendments to the Claims:**

This listing of claims will replace all prior versions and listings of claims in the application. In the listing below, inserted text is marked with underline, deleted text is marked with ~~strikethrough~~, and changes are identified by a vertical bar in the margin.

**Listing of Claims:**

1-64. (Canceled).

65. (New) A memory access method comprising:

detecting a write operation to a memory including a re-programmable non-volatile memory;

if an address of said write operation from a processor logic indicates a first address area of said non-volatile memory, then performing a first write operation of data to said non-volatile memory; and

if said address of said write operation from a processor logic indicates a second address area of said non-volatile memory, then performing a second write operation of data to said non-volatile memory according to a write operation speed that is different from the first write operation speed.

66. (New) A memory access method, according to claim 65,

wherein said first write operation is a fast write operation which is shorter time than a predetermined time to write said non-volatile memory; and

wherein said second write operation is a slow write operation which is executed full of said predetermined time to write said non-volatile memory.

67. (New) A memory access method comprising:

detecting a write operation to a non-volatile memory;

determining an access mode of said non-volatile memory corresponding to a mode register for controlling said non-volatile memory, if said access mode is a first mode, then

performing a fast write operation of data to said non-volatile memory, if said access mode is a second mode, then performing a slow write operation of data to said non-volatile memory,

if said access mode is a third mode write operation, then:

if an address of said non-volatile memory from a processing logic is indicated a first address area, then said non-volatile memory is executed said fast write operation of data,

if an address of said non-volatile memory is indicate a second address area, then said non-volatile memory is executed said slow write operation of data; and

if said access mode is a fourth mode, then performing a cache write operation of data to a cache memory comprised a random access memory based on an exception handler routine.

68. (New) A memory access method, according to claim 67,

wherein if a cache line of said cache memory stores other data in said cache write operation of said data, said other data is written to said non-volatile memory and said data is written to said cache line of said cache memory.

69. (New) A memory access method, according to claim 67,

wherein said mode register is indicated access mode for said non-volatile memory.

70. (New) A memory access method, according to claim 68,

wherein said slow write operation has a predetermined write time to said non-volatile memory; and

wherein said fast write operation has a write time shorter than said predetermined time of said slow write time.

71. (New) A memory access method, according to claim 67,

wherein said first address area and said second address area is indicated in a register.

72. (New) A memory access method according to claim 65, wherein detecting a write operation to the re-programmable non-volatile memory is based on identifying the write operation as directed to a predetermined address space that corresponds to the re-programmable non-volatile memory.

73. (New) A data processing unit comprising:

memory, including a re-programmable non-volatile memory; and

control logic configured for detecting a write operation to the memory and for performing said write operation according to an operation mode in which the control logic determines if an address of said write operation from a processor logic indicates a first address area of said non-volatile memory and performs a first write operation of data to said non-volatile memory, and if said address of said write operation from a processor logic indicates a second address area of said non-volatile memory, then performs a second write operation of data to said non-volatile memory.

74. A data processing unit according to claim 73, wherein the control logic detects a write operation to the re-programmable non-volatile memory by identifying the write operation as directed to a predetermined address space that corresponds to the re-programmable non-volatile memory.